REMARKS

This communication is a full and timely response to the non-final Office Action dated August 1, 2008. Claims 7-19 remain pending, where claims 1-6 were previously canceled. By this communication, claims 9 and 11 are amended and claims 16-19 are added. Support for the amended subject matter can be found, for example, at page 4, lines 11-17 of Applicants' original disclosure.

As a preliminary matter, Applicants appreciate the acknowledgement that claims 14 and 15 are allowed and that claims 9-12 recite allowable subject matter. Also, Applicants thank the Examiner for the granting of an interview on December 30, 2008. During the interview, Applicants' representative and the Examiner discussed the applied references under 35 U.S.C. §103. No agreement was reached.

In numbered paragraph 3 on page 2 of the Office Action, claims 7, 8, and 13 stand rejected under 35 U.S.C. §103(a) for alleged unpatentability over *Shimizu et al.* (USPN 6,201,696) in view of *Nidan et al.* (U.S. Patent Pub No. 2002/0005072). Applicants respectfully traverse this rejection.

As discussed in a previous response, Figures 1a through 6 illustrate an exemplary power semiconductor module that includes a substrate 2 sandwiched between a bottom metallization layer 3 and a top metallization layer 4. Both the top and bottom metallization layers 3 and 4 cover only a portion of the respective surface of the ceramic substrate 2, so that first corners 24 and second corners 23 are formed by the top and bottom metallization layers, respectively. A polyamide 5 is applied in the corners 24 and in the junction between the metallization layer 4 and ceramic substrate 2 such that these gaps are filled with insulating material.

Independent claims 7 and 13 broadly encompass the aforementioned features. For example, claim 7 recites the following:

> 7. A power semiconductor module, comprising:
> an electrically insulating substrate;
> a first electrically conductive layer disposed on at least one portion of a top surface of said electrically insulating substrate, so as to selectively expose at least one peripheral top region of said electrically insulating substrate;
> at least one semiconductor power chip mounted on said first electrically conductive layer;
> a first electrically insulating material disposed in a corner region formed by said first electrically conductive layer and said peripheral region of said electrically insulating substrate;
> a second insulating material at least partially embedding said semiconductor power chip, said electrically insulating substrate, said first electrically conductive layer, and said first electrically insulating material;
> wherein the first electrically insulating material is a polyimide, and the surface of the first electrically insulating material disposed in the corner region formed by said first electrically conductive layer and said peripheral region of said electrically insulating substrate is concave-shaped.

Claim 13 recites:

> 13. A power semiconductor module comprising:
> an electrically insulating substrate;
> a first electrically conductive layer disposed on at least one portion of a top surface of said electrically insulating substrate, so as to selectively expose at least one peripheral top region of said electrically insulating substrate;
> at least one semiconductor power chip mounted on said first electrically conductive layer;
> a first electrically insulating material disposed in a corner region formed by said first electrically conductive layer and said peripheral region of said electrically insulating substrate;
> a second insulating material at least partially embedding said semiconductor power chip, said electrically insulating substrate, said first electrically conductive layer, and said first electrically insulating material;
> wherein the first electrically insulating material is a polyimide, and the surface of the first electrically insulating material disposed in the corner region formed by said first electrically conductive layer and said peripheral region of said electrically insulating substrate is concave-shaped,
> wherein the first electrically insulating material fills gaps in a junction between the first electrically conductive layer and said electrically insulating substrate.

The Examiner alleges that *Shimizu* discloses every element recited in Applicants' claims except a first electrically insulating material that is a polyimide.

Nidan is relied upon in an effort to remedy this deficiency. Applicants respectfully submit, however, that the combination of these references does not establish a *prima facie* case of obviousness.

Nidan discloses a pressure sensor device having a sensor chip 4 with a diaphragm 5 formed on a main surface. The sensor chip 4 has electrode pads on the main surface. An electric signal generated by the sensing portion is transmitted to an external circuit connected to leads 2 through the electrode pads, the bumps 8 and the leads 2. The leads are insulated from metallic stems 1 to which they are attached. The diaphragm 5 constitutes a sensing portion in which piezo-resistors are formed. The piezo-resistors change in resistance in accordance with deformation of the diaphragm 5 by pressure applied to the diaphragm. A resin member 30 can be disposed on the diaphragm 5 between the sensor chip 4 and the stems 1 as protection member that transmits pressure to the diaphragm 5. The selection of the resin member 30 is selected based on the hardness of the material. *See* pgphs [0045], [0047], [0070], and [0071].

In Applicants' claimed embodiment, the polyimide has a low viscosity so that the material can fill any air gaps between the layers. *Nidan*, in contrast, discloses the use of a polyimide material with a high viscosity as a filler between a sensor chip and a stem so that the material does not flow out from between the chip and the stem.

One of ordinary skill would not have looked to *Nidan* to remedy the deficiencies of *Shimizu* as alleged. For one, *Nidan* is not directed to a power semiconductor device, but rather a pressure sensor. As such, there is seemingly no nexus between the two devices or disclosures that would lead one of ordinary skill to

combine their respective teachings. Stated differently, neither does the references nor the Examiner allege the existence of a technical rationale explaining why one of ordinary skill starting with a power semiconductor device as described by *Shimizu*, would modify this device with the teachings of *Nidan*. Particularly, there appears to be no rational basis for modifying the power semiconductor of *Shimizu* with the resin member of *Nidan* so that pressure can be transferred from one layer of the power semiconductor to another.

Applicants respectfully submit that if any rationale exists it is improperly derived from Applicants' own disclosure through hindsight reasoning. As a result, a *prima facie* case of obviousness has not been established.

The Office is reminded that the Examiner has the initial burden of establishing a **factual basis** to support the legal conclusion of obviousness. In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992). For rejections under 35 U.S.C. § 103(a) based upon a combination of prior art elements, in KSR Int'l v. Teleflex Inc., 127 S.Ct. 1727, 1741, 82 USPQ2d 1385, 1396 (2007), the Supreme Court stated that "a patent composed of several elements is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art." "Rejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some **articulated reasoning with some rational underpinning** to support the legal conclusion of obviousness." In re Kahn, 441 F.3d 977, 988, 78 USPQ2d 1329, 1336 (Fed. Cir. 2006) (emphasis added). For at least the foregoing reasons, withdrawal of this rejection is respectfully requested.

Claims 16-19 are newly added. These claims are distinguishable over the applied references based on their dependency from independent claims 7 and 13, and because of the additional elements recited therein. Thus, favorable consideration and examination are respectfully requested.

Conclusion

Based on at least the foregoing amendments and remarks, Applicants submit that claims 7-19 are allowable, and this application is in condition for allowance. In the event any issues remain, the Examiner is invited to contact Applicants' representative identified below.

Respectfully submitted,

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